In re Application of:
Frank K Baker Jr., et al.
Serial No.: 09/772,830
Filed: Jan. 30, 2001
For: A MEMORY SYSTEM AND METHOD OF ACCESSING THEREOF

April 14, 2005

Art Unit: 2188
Examiner: Mehdi Namazi
Docket No.: SC11150TH

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SECOND APPEAL BRIEF (AS AMENDED)

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent.

This brief has been modified in response to the Notification of Non-Compliant Appeal Brief Filed on March 15, 2006.

No fees are believed to be required for this Second Appeal Brief since an Appeal Brief for this application was filed on February 10, 2005 (First Appeal Brief) and such fees were paid at that time. However, if any additional fees are needed for this Brief or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079.

REAL PARTY IN INTEREST

The present application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., with its headquarters in Austin Texas.

RELATED APPEALS AND INTERFERENCES

This application was appealed for the first time in a Notice of Appeal filed December 10, 2004. An Appeal Brief (First Appeal Brief) was filed by Applicants on February 10, 2005 for that appeal.

Regarding the First Appeal, prosecution was reopened by the Second Final Office Action of July 28, 2005 (Second Final Office Action). The rejections from the Second Final Office Action are being appealed in this appeal brief.

STATUS OF CLAIMS

Claims 1-4, 6-10, and 12-26 are pending.

Claim 15 has been allowed.

Claims 1-4, 6-10, 12-14, and 16-26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno, U.S. Patent No. 6,105,114 (Okuno) in view of Morgan, U.S. Patent No. 6,083,271 (Morgan) as set forth in the Second Final Office Action of July 28, 2005 (Second Final Office Action).

The rejection of claims 1-4, 6-10, and 12-14, and 16-26 are being appealed.

STATUS OF AMENDMENTS

There have been no amendments made to the claims subsequent to the final rejection.

SUMMARY OF THE INVENTION

Independent claim 1 recites a memory system. The memory system includes an array of addressable storage elements arranged in a plurality of rows and a plurality of columns. The array of addressable storage elements includes a plurality of nonvolatile memory cells. The memory system includes decoding circuitry coupled to the array of addressable storage elements. The decoding circuitry, responsive to decoding a first

element address, to access a first storage element of a first row of the plurality of rows, and the decoding circuitry, responsive to decoding a second element address consecutive to the first element address, to access a second storage element of a second row of the plurality of rows. The second row of the plurality of rows is different from the first row of the plurality of rows. The first address comprises a group of bits. The second address comprises a group of bits. The decoding circuitry includes a row decoder and a column decoder. The row decoder is operable responsive to a first portion of the group of bits of the first address and the second address. The column decoder is operable responsive to a second portion of the group of bits of the first address and the second address. A bit of the second portion is more significant than a bit of the first portion.

In one example set forth in the specification of the present application, the memory system includes an array (210) of addressable storage elements (212) arranged in a plurality of rows and a plurality of columns. See Figure 2. The array of addressable storage elements includes a plurality of nonvolatile memory cells. Page 3, lines 18-19. The memory system includes decoding circuitry coupled to the array of addressable storage elements. (230, 220) The decoding circuitry, responsive to decoding a first element address, to access a first storage element of a first row of the plurality of rows, and the decoding circuitry, responsive to decoding a second element address consecutive to the first element address, to access a second storage element of a second row of the plurality of rows. Page 3, line 29 – page 4, line 9. The second row of the plurality of rows is different from the first row of the plurality of rows. The first address comprises a group of bits. The second address comprises a group of bits. The decoding circuitry includes a row decoder (230) and a column decoder (220). The row decoder is operable responsive to a first portion of the group of bits (the bits of A0 and A1) of the first address and the second address. The column decoder is operable responsive to a second portion of the group of bits (the bits of A2 and A3) of the first address and the second address. A bit of the second portion is more significant than a bit of the first portion. See Figure 2 and page 3, line 14 - page 4 line 9.

Claim 6 recites a memory system. The memory system includes an array of storage elements arranged in a plurality of rows and a plurality of columns. Each of the storage elements includes an input and an output. Each of the storage elements corresponds to a numeric address comprising more significant bits and less significant bits. The array of storage elements comprises a plurality of nonvolatile memory cells. The memory system includes a column decoder coupled to the outputs of the storage elements of each of the plurality of columns. The column decoder is operable responsive to at least one of the more significant bits. The memory system includes a row decoder

coupled to the inputs of the storage elements of each of the plurality of rows. The row decoder is operable responsive to at least one of the less significant bits.

In one example set forth in the specification of the present application, the memory system includes an array (210) of storage elements (212) arranged in a plurality of rows and a plurality of columns. See Figure 2. Each of the storage elements includes an input and an output. Page 10, lines 4-6. Each of the storage elements corresponds to a numeric address comprising more significant bits and less significant bits. Page 3, lines 19-28. The array of storage elements comprises a plurality of nonvolatile memory cells. Page 3, lines 17-19. The memory system includes a column decoder (220) coupled to the outputs of the storage elements of each of the plurality of columns. The column decoder is operable responsive to at least one of the more significant bits (the bits of A2 and A3). The memory system includes a row decoder (230) coupled to the inputs of the storage elements of each of the plurality of rows. The row decoder is operable responsive to at least one of the less significant bits (the bits of A1 and A2).

Claims 14 recites an embedded control system. The control system includes a processor and a memory system coupled to the processor. The memory system includes an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. The control system includes decoding circuitry including a column decoder and a row decoder. The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. Each address includes a group of bits. The row decoder is operable responsive to a first portion of the group of bits. The column decoder is operable responsive to a second portion of the group of bits. A bit of the second portion is more significant than a bit of the first portion.

In one example set forth in the specification of the present application, the embedded control system (300) includes a processor (301) and a memory system (302) coupled to the processor. The memory system includes an input to receive an address signal from the processor, an output to send addressed information to the processor, and a

plurality of blocks (BLK1 and BLK2). Page 4, lines 11-14. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. Page 5, lines 4-11. The control system includes decoding circuitry including a column decoder 320 and a row decoder (330). The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. See Figure 3. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. See Figure 3. Page 5, line 12- page 6, line 2. Each address includes a group of bits. The row decoder is operable responsive to a first portion of the group of bits. The column decoder is operable responsive to a second portion of the group of bits. Page 5, line 12 – page 6, line 2. A bit of the second portion is more significant than a bit of the first portion. See Figure 7 and page 6, lines 8-28.

Claim 16 recites a method of accessing a memory system. The memory system includes an array of addressable storage elements arranged in a plurality of rows and a plurality of columns. The array of addressable storage elements includes a plurality of nonvolatile memory cells. The method includes decoding a first element address. The method also includes accessing, responsive to the first element address, a first storage element of a first row of the plurality of rows. The method also includes decoding a second element address, the second element address consecutive to the first element address. The method still further includes accessing, responsive to the second element address, a second storage element of a second row of the plurality of rows. The second row of the plurality of rows is different from the first row of the plurality of rows. The first element address includes a group of bits. The decoding the first element address further includes decoding a first portion of the group of bits by a row decoder and decoding a second portion of the group of bits by a column decoder. A bit of the second portion is more significant than a bit of the first portion.

In one example set forth in the specification of the present application, the memory system includes an array (210) of addressable storage elements (212) arranged in a plurality of rows and a plurality of columns. The array of addressable storage elements includes a plurality of nonvolatile memory cells. Page 3, lines 17-19. The method includes decoding a first element address. The method also includes accessing,

responsive to the first element address, a first storage element of a first row of the plurality of rows. The method also includes decoding a second element address, the second element address consecutive to the first element address. The method still further includes accessing, responsive to the second element address, a second storage element of a second row of the plurality of rows. The second row of the plurality of rows is different from the first row of the plurality of rows. Page 3, line 29 - page 4, line 3. The first element address includes a group of bits. The decoding the first element address further includes decoding a first portion of the group of bits (the bits of A0 and A1) by a row decoder (230) and decoding a second portion of the group of bits (the bits of A2 and A3) by a column decoder (220). A bit of the second portion is more significant than a bit of the first portion.

Claim 22 recites an embedded control system. The control system includes a processor and a memory system coupled to the processor. The memory system includes an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. The control system includes decoding circuitry including a column decoder and a row decoder. The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. The address signal includes a group of bits. The row decoder is operable responsive to a first portion of the group of bits. The column decoder is operable responsive to a second portion of the group of bits. Each bit of the second portion is more significant than a least significant bit of the first portion.

In one example set forth in the specification of the present application, the embedded control system (300) includes a processor (301) and a memory system (302) coupled to the processor. The memory system includes an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks (BLK1 and BLK2). Page 4, lines 11-14. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality

of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. Page 5, lines 4-11. The control system includes decoding circuitry including a column decoder 320 and a row decoder (330). The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. See Figure 3. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. See Figure 3 and page 5, line 12 – page 6, line 2. The address signal includes a group of bits. The row decoder is operable responsive to a first portion of the group of bits. The column decoder is operable responsive to a second portion of the group of bits. Page 5, line 12 – page 6, line 2. Each bit of the second portion is more significant than a least significant bit of the first portion. See Figure 7 and page 6, lines 8-28.

Claim 25 recites a memory system that includes an input to receive an address signal, an output to send addressed information, and a plurality of blocks. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. Each of the plurality of blocks includes decoding circuitry including a column decoder and a row decoder. The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. The address signal includes a first group of bits representative of addresses of the plurality of rows and a second group of bits representative of addresses of pages within the plurality of rows. The second group includes a bit more significant than a bit of the first group. The address signal includes a third group of at least one bit representative of addresses of the plurality of blocks.

In one example set forth in the specification of the present application, the memory system includes an input to receive an address signal, an output to send addressed information, and a plurality of blocks. See Figure 3 and page 4, lines 10-14 and lines 25-30. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within

a plurality of pages. Page 4, lines 10-25 and page 5, lines 4-11. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. Page 5, lines 4-11. Each of the plurality of blocks includes decoding circuitry including a column decoder and a row decoder. Figure 3. The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. See Figure 3. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. Page 5, line 12 – page 6, line 7. The address signal includes a first group of bits representative of addresses of the plurality of rows and a second group of bits representative of addresses of pages within the plurality of rows. See Figure 7 and page 6, lines 8-28. The second group includes a bit more significant than a bit of the first group. The address signal includes a third group of at least one bit representative of addresses of the plurality of blocks. See Figure 7 and page 6, lines 8-28.

The specification and drawings may contain other embodiments of the claims not explicitly set forth above.

GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

1) Are claims 1-4, 6-10, 12-14, and 16-26 non obviousness under 35 U.S.C. 103(a) over Okuno, U.S. Patent No. 6,105,114 (Okuno) in view of Morgan, U.S. Patent No. 6,083,271 (Morgan).

2) Is claim 7 non obviousness under 35 U.S.C. 103(a) over Okuno in view of Morgan.

3) Is claim 12 non obviousness under 35 U.S.C. 103(a) over Okuno in view of Morgan.

4) Are claims 19 and 20 non obviousness under 35 U.S.C. 103(a) over Okuno in view of Morgan.

ARGUMENTS

Arguments for Ground 1

Claims 1-4, 6-10, 12-14, and 16-26 are non obviousness under 35 U.S.C. 103(a) over Okuno, U.S. Patent No. 6,105,114 (Okuno) in view of Morgan, U.S. Patent No. 6,083,271 (Morgan).

Independent Claim 1

Claim 1 is non obvious over Okuno and Morgan in that the Second Final Office Action has failed to set forth a proper motivation to modify the RAM of Okuno to provide a battery back up as taught by Morgan to teach the limitations of claim 1. Accordingly, the Second Final Office Action has not set forth a prima facie case for obviousness of claim 1.

Final Office Action Rejection

Claim 1 was rejected in Section 2 of the Second Final Office Action. Section 2 states that Okuno fails to teach a storage with a plurality of nonvolatile memory cells.

Section 2 of the Second Final Office Action states that Morgan discloses a RAM which does not permanently store information. However, the Second Final Office Action states that "to make a RAM memory non-volatile, it is known to connect a battery to RAM device (col. 6, lines 4-6)."

No motivation to combine Okuno and Morgan

In regards to the motivation to combine Okuno with Morgan, the Second Final Office Action states:

"it would have been obvious to one having ordinary skill … to incorporate the method of connecting a battery to a RAM device to make a non-volatile memory as taught by Morgan in corresponding to the storage device of Okuno. The modification would be obvious because of one … would be motivated to connect a battery to a RAM device in order to make the information stored in the battery-backed RAM device non-volatile (col. 6, lines 5-7)."

Applicants respectfully submit that making information stored in RAM non volatile is not a proper motivation under 35 USC 103(a) for one of skill in the art to add a battery backup system as taught by Morgan to the memory circuitry of Okuno. Nowhere in Okuno does it suggest that it would be desirable to non volatilely store the information in the memory array of Okuno.

Okuno teaches a transposition circuit for implementing a transforming coding technique using a two-dimensional discrete cosine transform for coding image data such

as MPEG data. Okuno, column 1, lines 8-25. Okuno implements a transposition memory circuit 1 for performing these operations. Okuno, column 7, lines 31-47. The circuit of Okuno is used for decoding multiple blocks of image data with a read and write operation being performed to each cell of array 2 for each block of data being processed. Okuno, column 7, line 31- column 8, line 36.

Nowhere in Okuno does it require circuit 1 of Okuno to be able to store data when the power is off, nor is there any suggestion of it being desirable to save the data in memory array 2. In fact, memory array 2 is not utilized to store data for any substantial period of time. Okuno appears to teach that data is only "stored" in memory array 2 during a cycling of the addresses as provided by counter 20 to perform the transposition operations. See Okuno, column 8, lines 9-13 and in general column 9, line 31 – column 10, line 34. Since circuit 1 is part of a coding system for image data, there is no need to store data in array 2 when circuit 1 does not have power in that circuit 1 would not be used to encode data when there is no power. Because there is no need to store data in array 2 of Okuno (other than for a short period of time during a transposition operation), there is no reason for one of skill in the art to modify Okuno to include the extra circuitry and complexity of a battery backed system as taught by Morgan.

Furthermore, Okuno teaches away from adding the additional circuitry of a battery backed system as taught by Morgan.

Okuno teaches (at many locations in its specification) that it is highly desirable to reduce circuit size and reduce power consumption. Okuno, column 1, lines 11-14; column 3, lines 57-64; column 4, lines 5-9 and lines 36-40; column 5, lines 12-14, lines 18-21, and lines 40-43; column 6, lines 8-10, lines 21-23, and lines 56-58; and column 11, lines 31-36. See as an example the Summary Of The Invention section of Okuno (column 4, lines 5-9) where it states "One object of the present invention is to provide a two-dimensional array transposition circuit having a reduced amount of memory for reducing circuit scale and power consumption."

Morgan on the other hand teaches that adding a battery back up for a RAM would require additional circuitry. For example, Column 6, lines 7-10 state that "An IC that incorporates the battery-backed RAM device requires two power domains one domain for its regular power DC source and another power domain for the battery." See also Column 6, lines 46-50 where it states that "cache memory 5 has a first power and ground domain for the D.C. power source while the circuit is in its nominal state and a second power and ground domain for the battery when the circuit is not powered on." In such a system, at least one or more I/O cells will be needed to provide both power and ground sources to the cache memory. Morgan, Column 7, lines 59-61. Furthermore, such a

system will require multiple pins for the multiple power and ground domains (Column 9, lines 3-5) as well as multiple busses (see Column 9, lines 26-33). See several examples in Columns 9-11 of Morgan of additional circuitry required for the battery back up system as taught by Morgan.

In addition to the extra circuitry required for a battery back up system, the battery itself will take up additional space and require charging, monitoring, voltage regulation, and power management circuitry and software. See Column 8, lines 9-27 of Morgan. Not only will the extra circuitry increase the size of the system of Okuno, it will also increase the power usage in operating this circuitry and performing software processing for the power management circuitry.

Furthermore, when DC power is removed, Morgan teaches the cache 5 will be consuming battery power when the circuit is not in operation. Morgan, Column 8, lines 15-18. Accordingly, providing a battery back up to the memory circuitry of Okuno would cause the memory circuitry of Okuno to consume more power. Increased power consumption is contrary to the desirability of reduced power consumption as taught by Okuno.

Claim 1 Summary

Thus, one of ordinary skill in the art would not be motivated to modify the memory array 2 of Okuno to provide a battery back up as taught by Morgan in that such a modification of would defeat the stated objectives of Okuno of reduced circuit size and reduced power consumption. Not only would implementing a battery back up as taught by Morgan increase the size of memory array 2 of Okuno due to the additional power domain circuitry, but it would also require the system of Okuno to include extra circuitry for charging, monitoring, voltage regulation, and power management circuitry and software as well. In addition, extra space would be needed for the battery itself. Furthermore, the memory array of Okuno would be consuming additional power when the system is not in operation. Since nowhere in Okuno does it teach or even suggest the desirability of having a non volatile memory, one of skill in the art would not be motivated to add the extra circuitry and increased power consumption of a battery backed system to Okuno, especially since Okuno teaches the desirability of less circuitry, less space, and reduced power consumption. Accordingly, claim 1 is allowable over Okuno and Morgan.

<u>Independent Claim 6</u>

For reasons similar to those set forth above for independent claim 1, independent claim 6 is non obvious over Okuno and Morgan in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Morgan to teach the limitations of

independent claim 6. Accordingly, independent claim 6 is allowable over Okuno and Morgan.

Independent Claim 14

For reasons similar to those set forth above for independent claim 1, independent claim 14 is non obvious over Okuno and Morgan in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Morgan to teach the limitations of independent claim 14. Accordingly, independent claim 14 is allowable over Okuno and Morgan.

Independent Claim 16

For reasons similar to those set forth above for independent claim 1, independent claim 16 is non obvious over Okuno and Morgan in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Morgan to teach the limitations of independent claim 16. Accordingly, independent claim 16 is allowable over Okuno and Morgan.

Independent Claim 22

For reasons similar to those set forth above for independent claim 1, independent claim 22 is non obvious over Okuno and Morgan in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Morgan to teach the limitations of independent claim 22. Accordingly, independent claim 22 is allowable over Okuno and Morgan.

Independent Claim 25

For reasons similar to those set forth above for independent claim 1, independent claim 25 is non obvious over Okuno and Morgan in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Morgan to teach the limitations of independent claim 25. Accordingly, independent claim 25 is allowable over Okuno and Morgan.

Dependent claims 2-4, 7-10, 12, 13, 17-21, 23, 24, and 26

Each dependent claim depends from an independent claim and is allowable for at least this reason.

Arguments for Ground 2

Dependent claim 7

Claim 7, is non obviousness over Okuno in view of Morgan under 35 U.S.C. 103(a).

Okuno and Morgan, either alone or in combination, do not disclose or suggest wherein the input of each of the storage elements is a control gate, all as recited by dependent claim 7.

Regarding claim 7, page 5 of the Second Final Office Action states that Okuno teaches where "the input of each of the storage elements is a control gate" and cites Figure 13 of Okuno for teaching the limitations of claim 7. Applicants respectfully submit that this is incorrect. Figure 13 of Okuno does not show a storage element of memory cell array 2 of Okuno, nor does Figure 13 of Okuno show a control gate. In contrast, Figure 13 of Okuno is a circuit for generating a control signal. Okuno, column 11, lines 1-2. Thus, Figure 13 of Okuno does not show where the input of each of the storage elements is a control gate.

Accordingly, claim 7 is allowable over Okuno and Morgan for at least this reason.

Arguments for Ground 3

Dependent claim 12

Regarding claim 12, a proper inherency position has not been established with respect to a limitation of claim 12 for an obviousness rejection under 35 U.S.C. 103(a) over Okuno in view of Morgan

Okuno and Morgan, either alone or in combination, do not disclose or suggest wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell, all as recited by claim 12.

Neither Okuno nor Morgan disclose a floating gate-type memory cell.

Regarding dependent claim 12, the first paragraph of page 6 of the Second Final Office Action states that "Okuno teaches wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell (it is inherent to use floating gate to detect the threshold voltage states in the cell transistor)."

Applicants respectfully submit that the first paragraph of page 6 is incorrect with respect to its discussion of claim 12. For example, Okuno does not teach non volatile memory cells. To further support the point that Okuno does not teach non volatile memory cells, see the last paragraph of page 4 of the Second Final Office Action where its states that Okuno "fails to teach a storage with plurality of nonvolatile memory cells." Accordingly, page 4 of the Second Final Office Action contradicts the first paragraph of page 6 of the Second Final Office Action on this point.

Also, Applicants respectfully submit that the statement "it is inherent to use floating gate to detect threshold states of the cell transistor," is also incorrect.

To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference. MPEP Section 2112, Subsection IV. Applicants respectfully submit that a floating gate-type cell is not necessarily present in memory array 2 of Okuno.

In the Response to Second Final Office Action mailed September 28, 2005, Applicants respectfully requested that the Examiner provide a basis in fact and/or technical reasoning to reasonably support the determination that a floating gate-type cell is necessarily present in the memory array of Okuno. See MPEP 2112, Subsection IV. As of this date, no such basis has been provided by the Examiner.

Accordingly, claim 12 is not non obvious under 35 U.S.C. 103(a) over Okuno in view of Morgan in that not all of the limitations of claim 12 are taught by Okuno and Morgan. See MPEP Section 2143.03 where it states "to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested in the prior art."

Because neither Okuno nor Morgan disclose a floating gate-type memory cell, nor is one inherent in the memory array of Okuno, claim 12 is allowable over Okuno and Morgan for at least this reason.

Arguments for Ground 4

Regarding claims 19 and 20, a proper inherency position has not been established with respect to limitations of claims 19 and 20 for an obviousness rejection under 35 U.S.C. 103(a) over Okuno in view of Morgan

Dependent claim 19

Okuno and Morgan, either alone or in combination, do not disclose or suggest wherein accessing a first storage element comprises initiating a first burst access, the first burst access comprising a plurality of bits. All as recited by dependent claim 19.

Page 6 of the Second Final Office Action states "Okuno teaches wherein accessing a first storage element comprises initiating a first burst access, the first burst access comprising a plurality of bits (it is inherent to access first row as a first burst)." No citation of Okuno is given in the Second Final Office Action for this proposition.

Applicants respectfully submit that the above proposition in the Second Final Office Action is incorrect in that nowhere does Okuno not teach initiating a burst access. Applicants respectfully request the Examiner cite where in Okuno it teaches "accessing a first storage element comprises initiating a first burst access, the first burst access comprising a plurality of bits."

Furthermore, Applicants respectfully request that the Examiner provide a basis in fact and/or technical reasoning to reasonably support the determination that Okuno teaches "initiating a first burst access."

Accordingly, dependent claims 19 and 20 are allowable for at least this reason.

Dependent claim 20

Okuno and Morgan, either alone or in combination, do not disclose or suggest wherein accessing a second storage element comprises initiating a second burst access different from the first burst access, the second burst access comprising a plurality of bits, all as recited by dependent claim 20.

Page 6 of the Second Final Office Action states "Okuno teaches wherein accessing a second storage element comprises initiating a second burst access different from the first burst access, the second burst access comprising a plurality of bits (it is inherent to access the second row as a second burst)." No citation of Okuno is given in the Second Final Office Action for this proposition.

Applicants respectfully submit that the above proposition in the Second Final Office Action is incorrect in that nowhere does Okuno not teach initiating a burst access. Applicants respectfully request the Examiner cite where in Okuno it teaches "accessing a second storage element comprises initiating a second burst access different from the first burst access, the second burst access comprising a plurality of bits."

Furthermore, Applicants respectfully request that the Examiner provide a basis in fact and/or technical reasoning to reasonably support the determination that Okuno teaches "initiating a second burst access."

Accordingly, dependent claims 20 is allowable for at least this reason.

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that the claims of the present application are allowable over the art cited during prosecution.

Respectfully submitted,

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Claims Appendix

1. (Previously Amended) A memory system comprising:

an array of addressable storage elements arranged in a plurality of rows and a plurality of columns, wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells; and

decoding circuitry coupled to the array of addressable storage elements, the decoding circuitry, responsive to decoding a first element address, to access a first storage element of a first row of the plurality of rows, and the decoding circuitry, responsive to decoding a second element address consecutive to the first element address, to access a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows;

wherein the first address comprises a group of bits;

wherein the second address comprises a group of bits;

wherein the decoding circuitry includes a row decoder and a column decoder;

wherein the row decoder is operable responsive to a first portion of the group of bits of the first address and the second address;

wherein the column decoder is operable responsive to a second portion of the group of bits of the first address and the second address, wherein a bit of the second portion is more significant than a bit of the first portion.

2. (Original) A memory system according to claim 1 wherein each of the storage elements stores one bit.

3. (Original) A memory system according to claim 1 wherein each of the storage elements stores a plurality of bits arranged as a word.

4. (Original) A memory system according to claim 1 wherein each of the storage elements stores a plurality of bits arranged as a page.

5. (Canceled).

6. (Previously Amended) A memory system comprising:

an array of storage elements arranged in a plurality of rows and a plurality of columns, each of the storage elements comprising an input and an output, each of the storage elements corresponding to a numeric address comprising more significant bits and less significant bits, wherein the array of storage elements comprises a plurality of nonvolatile memory cells;

a column decoder coupled to the outputs of the storage elements of each of the plurality of columns, the column decoder operable responsive to at least one of the more significant bits; and

a row decoder coupled to the inputs of the storage elements of each of the plurality of rows, the row decoder operable responsive to at least one of the less significant bits.

7. (Original) A memory system according to claim 6 wherein
the input of each of the storage elements is a control gate, and
the output of each of the storage elements is a drain.

8. (Original) A memory system according to claim 6 wherein each of the storage elements stores one bit.

9. (Original) A memory system according to claim 6 wherein each of the storage elements stores a plurality of bits arranged as a word.

10. (Original) A memory system according to claim 6 wherein each of the storage elements stores a plurality of bits arranged as a page.

11. (Canceled)

12. (Original) A memory system according to claim 6 wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell.

13. (Original) A memory system according to claim 6 wherein the at least one of the less significant bits comprises all of the less significant bits.

14. (Previously Amended) An embedded control system comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein each address comprises a group of bits;

wherein the row decoder is operable responsive to a first portion of the group of bits;

wherein the column decoder is operable responsive to a second portion of the group of bits, wherein a bit of the second portion is more significant than a bit of the first portion.

15. (Previously Amended) An embedded control system comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein the address signal comprises:

least significant bits representative of addresses of bits within a word,

next least significant bits representative of addresses of words within a page,

intermediate significant bits representative of addresses of the plurality of rows, the intermediate significant bits more significant than the next least significant bits,

more significant bits representative of addresses of pages within the plurality of rows, the more significant bits more significant than the intermediate significant bits, and

next more significant bits representative of addresses of the plurality of blocks, the next more significant bits more significant than the more significant bits.

16. (Previously Amended) A method of accessing a memory system, the memory system comprising an array of addressable storage elements arranged in a plurality of rows and a plurality of columns, wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells, the method comprising:

decoding a first element address;

accessing, responsive to the first element address, a first storage element of a first row of the plurality of rows;

decoding a second element address, the second element address consecutive to the first element address; and

accessing, responsive to the second element address, a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows;

wherein the first element address includes a group of bits;

wherein the decoding the first element address further includes decoding a first portion of the group of bits by a row decoder and decoding a second portion of the group of bits by a column decoder;

wherein a bit of the second portion is more significant than a bit of the first portion.

17. (Original) A method according to claim 16 wherein accessing a first storage element comprises reading a first page, the first page comprising a plurality of bits.

18. (Original) A method according to claim 17 wherein accessing a second storage element comprises reading a second page different from the first page, the second page comprising a plurality of bits.

19. (Original) A method according to claim 16 wherein accessing a first storage element comprises initiating a first burst access, the first burst access comprising a plurality of bits.

20. (Original) A method according to claim 19 wherein accessing a second storage element comprises initiating a second burst access different from the first burst access, the second burst access comprising a plurality of bits.

21. (Previously Added) The memory system of claim 6 wherein:
the numeric address comprises a group of bits;
the row decoder is operable responsive to a first portion of the group of bits;
the column decoder is operable responsive to a second portion of the group of bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion.

22. (Previously amended) An embedded control system comprising:
a processor; and
a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:
an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and
decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;
wherein:

the address signal comprises a group of bits;

the row decoder is operable responsive to a first portion of the group of bits;

the column decoder is operable responsive to a second portion of the group of bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion.

23. (Previously added) The memory system of claim 1 wherein each bit of the second portion is more significant than a least significant bit of the first portion.

24. (Previously added) The method of claim 16 wherein each bit of the second portion is more significant than a least significant bit of the first portion.

25. (Previously added) A memory system comprising an input to receive an address signal, an output to send addressed information, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page_address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein the address signal comprises:

a first group of bits representative of addresses of the plurality of rows,

a second group of bits representative of addresses of pages within the plurality of rows, wherein the second group includes a bit more significant than a bit of the first group;

a third group of at least one bit representative of addresses of the plurality of blocks.

26. (Previously added) The embedded control system of claim 14, wherein at least one bit of the group of bits is representative of addresses of the plurality of blocks.

Evidence Appendix

None

Related proceedings appendix

There are no decisions rendered by the Board in any related appeals including in the first Appeal of this application.